REMARKS

This communication is in response to the Non-Final Office Action of December 27, 2007.

In response to the 35 USC 102-103 claim rejections, Applicant has amended the claims to recite with more particularly that utilization is monitored by determining a percentage of clock cycles for which at least one stage in a graphics pipeline is stalled waiting for inputs from upstream stages. Support for this amendment is found in paragraphs [0032] –[0033]. As described in paragraph [0031], in a pipelined graphics system a block typically requires the output of one or more other stages as inputs in order to perform its function. When individual blocks become over-utilized they slow down the performance of downstream blocks. As described in paragraph [0032], if there is a high percentage of clock cycles for which one or more stages are held up waiting for the output of previous stages increasing the performance level may result in allowing prior blocks to keep up, thereby increasing the display rate.

Applicant has also amended the claims to clarify that the higher performance levels have a higher clock rate compared with lower performance levels. Consequently, an increase in performance level in response to an over-utilization condition results in an increase in a clock rate in the processor core clock domain.

The claimed invention directly monitors utilization of a graphics pipeline in regards to monitoring the percentage of clock cycles for which a graphics pipeline in stalled waiting for inputs from upstream stages. This direct measurement of graphics pipeline utilization permits the performance level to be precisely tuned.

In contrast, the cited art does not actively monitor a graphics pipeline. GIEMBOREK monitors software running on the CPU and various display mode settings to adjust clock rates. However GIEMBOREK does not monitor current conditions within a graphics pipeline and further GIEMBORK does not teach or suggest monitoring the percentage of clock cycles for which the graphics pipeline is stalled waiting for inputs from upstream stages to determine when to adjust performance levels. WILLIAMS and JUN also does not teach this function.

BOSE is a different field of art and actually teaches away from the claimed invention. One of ordinary skill in the art would understand that a graphics pipeline functions differently from a superscalar processor. In particular, stalling is described in the superscalar processor of BOSE as being completely unrelated to waiting for inputs from upstream stages. The superscalar

processor of BOSE includes separate clocks for different units (CLK-I for an I-unit and CLK-E for an E-unit). In BOSE the detection of a stall in an E-unit results in an adjustment down of the clock speed in the upstream I-unit to "reduce (or cut off)" the rate at which instructions are received by the stalled E-unit (column 6, lines 45-46, "stall bit 130 is used to adjust down the clock speed'). Thus in BOSE a stall in a stage results in the stage requesting the upstream unit to reduce its clock rate to cut down the rate at which instructions are received. In contrast, in the claimed invention, the performance level (and hence clock rate) is increased in response to detecting a stall because in a graphics pipeline a stage can become stalled waiting for data from an upstream stage such that it is beneficial to increase the clock rate. It is therefore respectfully submitted that BOSE cannot be properly combined with GIEMBOREK and WILLIAMS, since BOSE teaches reducing clock rate in response to detecting a stall, which is contrary to specific claim limitations regarding the increase in performance level (and clock rate) when there is an over-utilization condition. That is, the combination of references, when fairly interpreted, fails to teach all of the elements of the claimed invention. Moreover, one of ordinary skill in the art would not be motivated to make the combination in light of the fundamental difference in operation of the different types of processors described in the cited references.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 50-1283.

Respectfully submitted,
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